coolaudio

4096-Stage Low-Noise BBD Analog Delay Line

V3205D/SD

General Description

The V3205D/SD is a 4096-stage low voltage operation (VDD = 5 V) BBD that provides a signal delay of up to 204.8 ms at clock frequency 10 KHz and is suitable for use as reverberation effect of audio equipments such as portable stereo and radio cassette recorders which need low voltage and long delay time since S/N is 60 dB in spite of many stages.

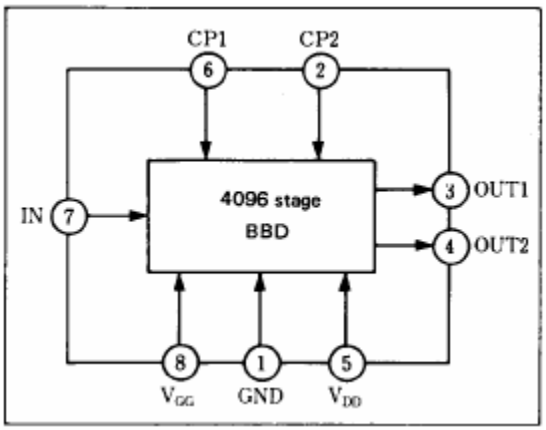
Features:

- Variable delay of audio signals: 20.48 ms ~ 204.8 ms.
- Wide power supply voltage: 4 ~ 8 V.
- No insertion noise: Li = 0 dB typ.
- Wide dynamic range: S/N = 60 dB.
- N Channel silicon gate process.
- Special 8-Lead Dual-In-Line plastic Package.

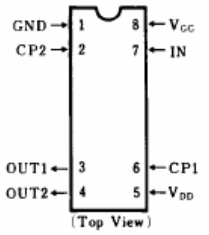
Applications

- Reverberation and echo effects of audio equipment such as radio cassette recorder, car radio, portable radio, portable stereo, echo microphone and pre-taped musical accompaniment (Karaoke), etc.
- Sound effect of electronic musical instrument.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication system.

Block Diagram

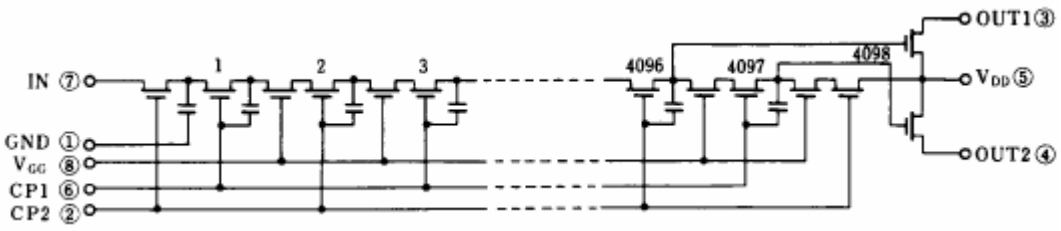


Pin Configuration



No.	Symbol	Type	Description
1	GND	P	Ground
2	CP2	I	The second clock input
3	OUT1	O	Signal output, delayed 4096 times
4	OUT2	O	Signal output, delayed 4097 times
5	V_{DD}	P	Power
6	CP1	I	The first clock input
7	IN	I	Analog signal input
8	V_{GG}	I	Bias voltage input ($^{14}/_{15}V_{DD}$)

Circuit Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	+5, $^{14}/_{15}V_{DD}$	V
Signal Delay Time	t_D	20.48 ~ 204.8	ms
Total Harmonic Distortion	THD	0.8	%
Signal to Noise Ratio	S/N	60	dB

Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Rating	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_i	-0.3 ~ +11	V
Output Voltage	V_O	-0.3 ~ +11	V
Operation Ambient Temp.	T_{opr}	-20 ~ +60	°C
Storage Temp.	T_{stg}	-55 ~ +125	°C

Operating Condition (Ta = 25 °C)

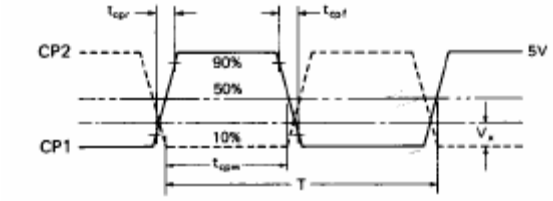
Item	Symbol	Condition	Min.	Typ.	Max	Unit
Drain Supply Voltage	V_{DD}		+4	+5	+8	V
Gate Supply Voltage	V_{GG}			$^{14}/_{15}V_{DD}$		V
Clock Voltage High	V_{CPH}			V_{DD}		V
Clock Voltage Low	V_{CPL}		0		+0.5	V
Clock frequency	f_{CP}		10		100	kHz
Clock Pulse Width *1	t_{CPW}				0.5T*2	
Clock Rise Time *1	t_{CPr}				500	ns
Clock fall Time *1	t_{CPf}				500	ns
Clock Input Capatence	C_{CP}				2800	pF
Clock Cross Point	V_X		0		0.3 V_{CPH}	V

Electrical Characteristics

(Ta = 25 °C, V_{DD} = VCPH = 5 V, VCPL = 0 V, VGG = 14/15 VDD, RL=100 kΩ)

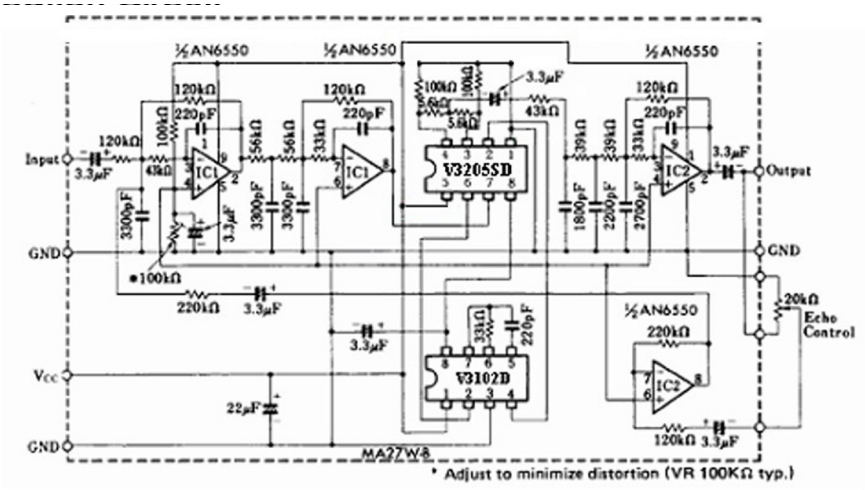
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay time	t_O		20.48		204.8	ms
Input Signal Freq.	f_i	fCP = 40 kHz, Output Attenuation ≤ 3dB	6			kHz
Input Signal Swing	V_i	THD = 2.5%	0.36			Vrms
Insertion Loss	L_i	fCP = 40 kHz, fi = 1 kHz	-4	0	4	dB
Total Harm. Dist.	THD	fCP = 40 kHz, fi = 1 kHz, Vi = 0.25 Vrms		0.8	2.5	%
Output Noise Voltage	V_{ON}	tCP = 100 kHz, Weighted by "A" curve			0.35	mV_{rms}
Signal to Noise Ratio	S/N			60		dB

*1 Clock Pulse Waveform



*2 T = $1/f_{CP}$ (Clock Period)

Application Circuit



Mechanical Specification